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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/823,076	04/13/2004	Joung-yeal Kim	5649-1229	3985

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EXAMINER	
MERANT, GUERRIER	

ART UNIT	PAPER NUMBER
2117	

MAIL DATE	DELIVERY MODE
10/28/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/823,076	KIM ET AL.	
	Examiner	Art Unit	
	Guerrier Merant	2117	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 July 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,10-13,21 and 37-41* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3, 10-13, 21 and 37-41* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. Applicant's amendment filled 07/18/08, with respect to claims 1-3, 10-13, 21 and 37-41 have been fully considered but they are not persuasive.

Response to Arguments

2. As per the 35 U.S.C. 112, second paragraph rejections, the Applicant argued that *"...in the embodiment illustrated in Figure 3 of the present application, the number of word lines* ***n = 2,*** *and the number of column selecting lines* ***m = 4****. As such, as correctly noted by the Examiner, the "nm memory cell arrays" and the "nm bit comparison data" of Claim 1 refers to the product or multiplication of the number of word lines n by the number of column selecting lines m. Thus, in the example embodiment of Figure 3, nm = 8, as illustrated by the* ***8 memory cell region****".* The Examiner respectfully disagrees for the following reasons:

First of all, n and m are indefinite in the claims. The claims disclose n and m as any integers greater than 1.

Second of all, the claimed are directed to **a memory cell array** with row and column lines but not **a memory cell region** as argued by the Applicant.

Therefore, the Examiner maintains prior 35 U.S.C 112, second paragraph rejections of the claims.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1, 10-11, and 21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claims 1, 10-11, and 21: The claims identify "**nm**" as the number of memory cell arrays and then the same "**n**" and "**m**" are being identified as the number of word lines and column lines respectively.

Claims 1, 10-11 and 21 recites the limitation "y" in line 4. There is insufficient antecedent basis for this limitation in the claim.

Claims 2-3, 12-13 and 37-41 inherit the 35 U.S.C. 112, second paragraph issued of the independent claims 1, 10 and 21 by virtue of their dependency.

According to the Examiner's interpretation:

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-3, 10-13, 21, and 37-41 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (herein after AAPA) and further in view of Kim et al.

Claims 1-3: AAPA teaches a method for testing a semiconductor memory device including nm memory cell arrays for respectively outputting x-bit data when n word lines and m column selecting signal lines are selected wherein n, m, and x are integers greater than 1, wherein nm comprises n multiplied by m, and wherein y is less than nm, the method comprising: extending y-bit data received through y data I/O pads to (nmxx)-bit data to write the x-bit data to each of the nm memory cell arrays in a test data write step (e.g. [0011, lines last two sentences]); and comparing the x-bit data output from each of the nm memory cell arrays to generate nm-bit comparison result data (e.g. [0006] & ([0011], lines 18-26). But AAPA fails to explicitly teach sequentially outputting y-bit comparison result data selected by selecting, by y bits, the nm-bit comparison result data in response to a control signal to the y data I/O pads, respectively, in a test data read step. However, Kim et al teaches testing a semiconductor device wherein a comparison system (e.g. items 501-508, fig. 4) compares writing data with read data and sequentially outputs the comparison result data through a selected I/O pad (e.g. col. 4, lines 50-67;col. 5, lines 4—29). Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to improve the teaching of AAPA with the one taught by Kim et al in order to reduce testing time (e.g. col. 2, lines 5-23- Kim et al).

Claims 10, 39-41: AAPA teaches a method for testing a semiconductor memory device including nm memory cell arrays for respectively outputting x-bit data when n word lines and m

column selecting signal lines are selected wherein n, m, and x are integers greater than 1, wherein nm comprises n multiplied by m, and wherein y is less than nm, the method comprising: extending y-bit data received through y data I/O pads to (nmxx)-bit data to write the x-bit data to each of the nm memory cell arrays wherein nm is integer time as greater as y in a test data write step (e.g. [0011, lines last two sentences]); and comparing the x-bit data output from each of the nm memory cell arrays to generate ran-bit comparison result data, grouping and outputting the ran-bit comparison result data into y groups by bit data generated with respect to corresponding n word lines or with respect to corresponding m column selecting signal lines in response to a control signal, and outputting y-bit comparison result data generated to the y data I/O pads in a test data read step (e.g. [0006] & ([0011], lines 18-26). But AAPA fails to explicitly teach sequentially outputting y-bit comparison result data selected by selecting, by y bits, the nm-bit comparison result data in response to a control signal to the y data I/O pads, respectively, in a test data read step. However, Kim et al teaches testing a semiconductor device wherein a comparison system (e.g. items 501-508, fig. 4) compares writing data with read data and sequentially outputs the comparison result data through a selected I/O pad (e.g. col. 4, lines 50-67;col. 5, lines 4—29). Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to improve the teaching of AAPA with the one taught by Kim et al in order to reduce testing time (e.g. col. 2, lines 5-23- Kim et al).

Claims 11-13: AAPA teaches a semiconductor memory device comprising nm memory cell arrays configured to respectively outputting x-bit data when n word lines and m column selecting signal lines are selected wherein n, m, and x are integers greater than 1 (e.g. items 1-8,

fig. 1), wherein nm comprises n multiplied by m, and wherein y is less than nm; a test data write circuit (e.g. item 18, fig. 1) configured to extend y-bit data received through y data I/O pads to (nmxx)-bit data to write the x-bit data to each of the nm memory cell arrays in a test data write step (e.g. [0011, lines last two sentences]); and test data read circuit (e.g. fig. 2) configured to compare the x-bit data output from each of the nm memory cell arrays to generate nm-bit comparison result data, and output y-bit comparison result data to the y data I/O pads (e.g. [0006] & ([0011], lines 18-26). But AAPA fails to explicitly teach sequentially outputting y-bit comparison result data selected by selecting, by y bits, the nm-bit comparison result data in response to a control signal to the y data I/O pads, respectively, in a test data read step. However, Kim et al teaches testing a semiconductor device wherein a comparison system (e.g. items 501-508, fig. 4) compares writing data with read data and sequentially outputs the comparison result data through a selected I/O pad (e.g. col. 4, lines 50-67;col. 5, lines 4—29). Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to improve the teaching of AAPA with the one taught by Kim et al in order to reduce testing time (e.g. col. 2, lines 5-23- Kim et al).

Claims 21, 37-38: AAPA teaches a semiconductor memory device comprising nm memory cell arrays configured to respectively outputting x-bit data when n word lines and m column selecting signal lines are selected wherein n, m, and x are integers greater than 1, wherein nm comprises n multiplied by m, and wherein y is less than nm (e.g. items 1-8, fig. 1);

a test data write circuit (e.g. item 18, fig. 1) configured to extend y-bit data received through y data I/O pads to (nmxx)-bit data to write the x-bit data to each of the nm memory cell arrays wherein nm is integer times as greater as y (e.g. [0011, lines last two sentences]);

and test data read circuit (e.g. fig. 2) configured to compare the x-bit data output from each of the nm memory cell arrays to generate nm-bit comparison result data, and output y-bit comparison result data to the y data I/O pads (e.g. [0006] & ([0011], lines 18-26). But AAPA fails to explicitly teach sequentially outputting y-bit comparison result data selected by selecting, by y bits, the nm-bit comparison result data in response to a control signal to the y data I/O pads, respectively, in a test data read step. However, Kim et al teaches testing a semiconductor device wherein a comparison system (e.g. items 501-508, fig. 4) compares writing data with read data and sequentially outputs the comparison result data through a selected I/O pad (e.g. col. 4, lines 50-67;col. 5, lines 4—29). Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to improve the teaching of AAPA with the one taught by Kim et al in order to reduce testing time (e.g. col. 2, lines 5-23- Kim et al).

Conclusion

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period

will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Exr. Merant Guerrier whose telephone number is (571) 270-1066. The examiner can normally be reached Monday through Thursday from 10: 30 a.m. to 3:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis Jacques, can be reached on (571) 272-6962. Draft or Informal faxes, which will not be entered in the application, may be submitted directly to the examiner at (571) 270-2066.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Guerrier Merant
10/20/08

/JACQUES H LOUIS-JACQUES/

Supervisory Patent Examiner, Art Unit 2100